

FEATURES

- Fast slew rate: 22 V/ μ s typical
- Settling time (0.01%): 1.2 μ s maximum
- Offset voltage: 300 μ V maximum
- High open-loop gain: 1000 V/mV minimum
- Low total harmonic distortion: 0.002% typical
- Improved replacement for AD712, LT1057, OP215, TL072, and MC34082

APPLICATIONS

- Output amplifier for fast DACs
- Signal processing
- Instrumentation amplifiers
- Fast sample-and-holds
- Active filters
- Low distortion audio amplifiers
- Input buffer for ADCs
- Servo controllers

GENERAL DESCRIPTION

The OP249 is a high speed, precision dual JFET op amp, similar to the popular single op amp, the OP42. The OP249 outperforms available dual amplifiers by providing superior speed with excellent dc performance. Ultrahigh open-loop gain (1 kV/mV minimum), low offset voltage, and superb gain linearity makes the OP249 the industry's first true precision, dual high speed amplifier.

With a slew rate of 22 V/ μ s typical and a fast settling time of less than 1.2 μ s maximum to 0.01%, the OP249 is an ideal choice for high speed bipolar DAC and ADC applications. The excellent dc performance of the OP249 allows the full accuracy of high resolution CMOS DACs to be realized.

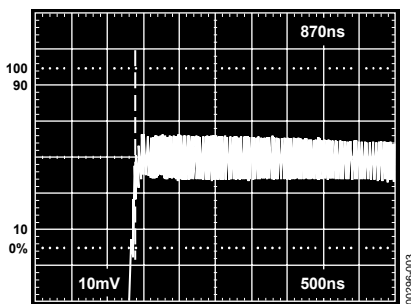


Figure 3. Fast Settling (0.01%)

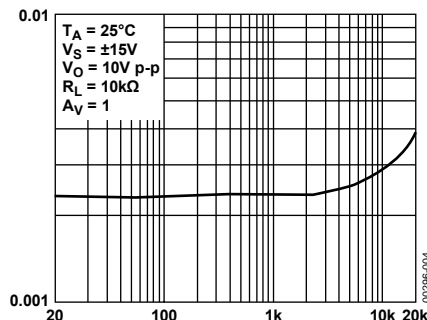


Figure 4. Low Distortion, $A_V = 1$, $R_L = 10\text{ k}\Omega$

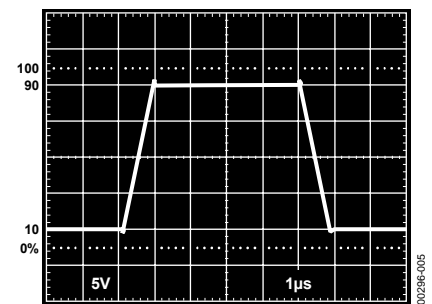


Figure 5. Excellent Output Drive, $R_L = 600\ \Omega$

PIN CONFIGURATIONS

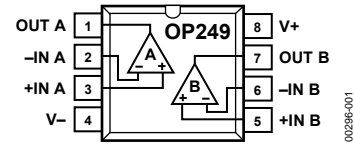


Figure 1. 8-Lead CERDIP (Q-8) and 8-Lead PDIP (N-8)

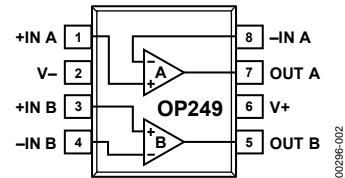


Figure 2. 8-Lead SOIC (R-8)

Symmetrical slew rate, even when driving large load, such as, 600 Ω or 200 pF of capacitance and ultralow distortion, make the OP249 ideal for professional audio applications, active filters, high speed integrators, servo systems, and buffer amplifiers.

The OP249 provides significant performance upgrades to the TL072, AD712, OP215, MC34082, and LT1057.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	OP249A			OP249F			Unit
			Min	Typ	Max	Min	Typ	Max	
Offset Voltage	V_{OS}			0.2	0.5		0.2	0.7	mV
Long Term Offset Voltage ¹	V_{OS}				0.8			1.0	mV
Offset Stability				1.5			1.5		$\mu\text{V}/\text{month}$
Input Bias Current	I_B	$V_{CM} = 0\text{ V}$, $T_A = 25^\circ\text{C}$		30	75		30	75	pA
Input Offset Current	I_{OS}	$V_{CM} = 0\text{ V}$, $T_A = 25^\circ\text{C}$		6	25		6	25	pA
Input Voltage Range ²	IVR			12.5			12.5		V
			± 11			± 11			V
				-12.5			-12.5		V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11\text{ V}$	80	90		80	90		dB
Power-Supply Rejection Ratio	PSRR	$V_S = \pm 4.5\text{ V}$ to $\pm 18\text{ V}$		12	31.6		12	50	$\mu\text{V}/\text{V}$
Large Signal Voltage Gain	A_{VO}	$V_O = \pm 10\text{ V}$, $R_L = 2\text{ k}\Omega$	1000	1400		500	1200		V/mV
Output Voltage Swing	V_O	$R_L = 2\text{ k}\Omega$		12.5			12.5		V
			± 12.0			± 12.0			V
				-12.5			-12.5		V
Short-Circuit Current Limit	I_{SC}	Output shorted to ground		36			36		mA
			± 20		± 50	± 20		± 50	mA
				-33			-33		mA
Supply Current	I_{SY}	No load, $V_O = 0\text{ V}$		5.6	7.0		5.6	7.0	mA
Slew Rate	SR	$R_L = 2\text{ k}\Omega$, $C_L = 50\text{ pF}$	18	22		18	22		V/ μs
Gain Bandwidth Product ³	GBW		3.5	4.7		3.5	4.7		MHz
Settling Time	t_S	10 V step 0.01% ⁴		0.9	1.2		0.9	1.2	μs
Phase Margin	Θ_M	0 dB gain		55			55		Degrees
Differential Input Impedance	Z_{IN}			$10^{12} 6$			$10^{12} 6$		ΩpF
Open-Loop Output Resistance	R_O			35			35		Ω
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		2			2		$\mu\text{V p-p}$
Voltage Noise Density	e_n	$f_o = 10\text{ Hz}$		75			75		$\text{nV}/\sqrt{\text{Hz}}$
		$f_o = 100\text{ Hz}$		26			26		$\text{nV}/\sqrt{\text{Hz}}$
		$f_o = 1\text{ kHz}$		17			17		$\text{nV}/\sqrt{\text{Hz}}$
		$f_o = 10\text{ kHz}$		16			16		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	i_n	$f_o = 1\text{ kHz}$		0.003			0.003		$\text{pA}/\sqrt{\text{Hz}}$
Voltage Supply Range	V_S		± 4.5	± 15	± 18	± 4.5	± 15	± 18	V

¹ Long-term offset voltage is guaranteed by a 1000 hour life test performed on three independent wafer lots at 125°C with LTPD of three.

² Guaranteed by CMR test.

³ Guaranteed by design.

⁴ Settling time is sample tested.

OP249

$V_S = \pm 15\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	OP249G			Unit
			Min	Typ	Max	
Offset Voltage	V_{OS}			0.4	2.0	mV
Input Bias Current	I_B	$V_{CM} = 0\text{ V}$, $T_A = 25^\circ\text{C}$		40	75	pA
Input Offset Current	I_{OS}	$V_{CM} = 0\text{ V}$, $T_A = 25^\circ\text{C}$		10	25	pA
Input Voltage Range ¹	IVR			12.5		V
			± 11			V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11\text{ V}$		-12.0		V
			76	90		dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5\text{ V}$ to $\pm 18\text{ V}$		12	50	$\mu\text{V/V}$
Large Signal Voltage Gain	A_{VO}	$V_O = \pm 10\text{ V}$; $R_L = 2\text{ k}\Omega$	500	1100		V/mV
Output Voltage Swing	V_O	$R_L = 2\text{ k}\Omega$		12.5		V
			± 12.0			V
Short-Circuit Current Limit	I_{SC}	Output shorted to ground		-12.5		V
				36		mA
			± 20		± 50	mA
				-33		mA
Supply Current	I_{SY}	No load; $V_O = 0\text{ V}$		5.6	7.0	mA
Slew Rate	SR	$R_L = 2\text{ k}\Omega$, $C_L = 50\text{ pF}$	18	22		V/ μs
Gain Bandwidth Product ²	GBW			4.7		MHz
Settling Time	t_S	10 V step 0.01%		0.9	1.2	μs
Phase Margin	θ_M	0 dB gain		55		Degree
Differential Input Impedance	Z_{IN}			$10^{12} \parallel 6$		$\Omega \parallel \text{pF}$
Open-Loop Output Resistance	R_O			35		Ω
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		2		μV p-p
Voltage Noise Density	e_n	$f_o = 10\text{ Hz}$		75		$\text{nV}/\sqrt{\text{Hz}}$
		$f_o = 100\text{ Hz}$		26		$\text{nV}/\sqrt{\text{Hz}}$
		$f_o = 1\text{ kHz}$		17		$\text{nV}/\sqrt{\text{Hz}}$
		$f_o = 10\text{ kHz}$		16		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	i_n	$f_o = 1\text{ kHz}$		0.003		$\text{pA}/\sqrt{\text{Hz}}$
Voltage Supply Range	V_S		± 4.5	± 15	± 18	V

¹ Guaranteed by CMR test.

² Guaranteed by design.

$V_S = \pm 15\text{ V}$, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ for F grade and $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ for A grade, unless otherwise noted.

Table 3.

Parameter	Symbol	Conditions	OP249A			OP249F			Unit
			Min	Typ	Max	Min	Typ	Max	
Offset Voltage	V_{OS}			0.12	1.0		0.5	1.1	mV
Offset Voltage Temperature Coefficient	TCV_{OS}			1	5		2.2	6	$\mu\text{V}/^\circ\text{C}$
Input Bias Current ¹	I_B			4	20		0.3	4.0	nA
Input Offset Current ¹	I_{OS}			0.04	4		0.02	1.2	nA
Input Voltage Range ²	IVR			12.5			12.5		V
			± 11			± 11			V
				-12.5			-12.5		
Common-Mode Rejection	CMR	$V_{CM} = \pm 11\text{ V}$	76	110		80	90		dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5\text{ V to } \pm 18\text{ V}$		5	50		7	100	$\mu\text{V}/\text{V}$
Large Signal Voltage Gain	A_{VO}	$R_L = 2\text{ k}\Omega; V_O = \pm 10\text{ V}$	500	1400		250	1200		V/mV
Output Voltage Swing	V_O	$R_L = 2\text{ k}\Omega$		12.5			12.5		V
			± 12			± 12			V
				-12.5			-12.5		
Supply Current	I_{SY}	No load, $V_O = 0\text{ V}$		5.6	7.0		5.6	7.0	mA

¹ $T_A = 85^\circ\text{C}$ for F grade; $T_A = 125^\circ\text{C}$ for A grade.

² Guaranteed by CMR test.

$V_S = \pm 15\text{ V}$, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$, unless otherwise noted.

Table 4.

Parameter	Symbol	Conditions	OP249G			Unit
			Min	Typ	Max	
Offset Voltage	V_{OS}			1.0	3.6	mV
Offset Voltage Temperature Coefficient	TCV_{OS}			6	25	$\mu\text{V}/^\circ\text{C}$
Input Bias Current ¹	I_B			0.5	4.5	nA
Input Offset Current ¹	I_{OS}			0.04	1.5	nA
Input Voltage Range ²	IVR			12.5		V
			± 11			V
				-12.5		V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11\text{ V}$	76	95		dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5\text{ V to } \pm 18\text{ V}$		10	100	$\mu\text{V}/\text{V}$
Large Signal Voltage Gain	A_{VO}	$R_L = 2\text{ k}\Omega; V_O = \pm 10\text{ V}$	250	1200		V/mV
Output Voltage Swing	V_O	$R_L = 2\text{ k}\Omega$		12.5		V
			± 12.0			V
				-12.5		V
Supply Current	I_{SY}	No load, $V_O = 0\text{ V}$		5.6	7.0	mA

¹ $T_A = 85^\circ\text{C}$.

² Guaranteed by CMR test.

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter ¹	Rating
Supply Voltage	±18 V
Input Voltage ²	±18 V
Differential Input Voltage ²	36 V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	
OP249A (Q)	−55°C to +125°C
OP249F (Q)	−40°C to +85°C
OP249G (N, R)	−40°C to +85°C
Junction Temperature Range	
OP249A (Q), OP249F (Q)	−65°C to +175°C
OP249G (N, R)	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

¹ Absolute maximum ratings apply to packaged parts, unless otherwise noted.

² For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 6. Thermal Resistance

Package Type	θ_{JA} ¹	θ_{JC}	Unit
8-Lead CERDIP (Q)	134	12	°C/W
8-Lead PDIP (N)	96	37	°C/W
8-Lead SOIC (R)	150	41	°C/W

¹ θ_{JA} is specified for worst-case mounting conditions, that is, θ_{JA} is specified for device in socket for CERDIP and PDIP packages; θ_{JA} is specified for device soldered to printed circuit board for SOIC package.

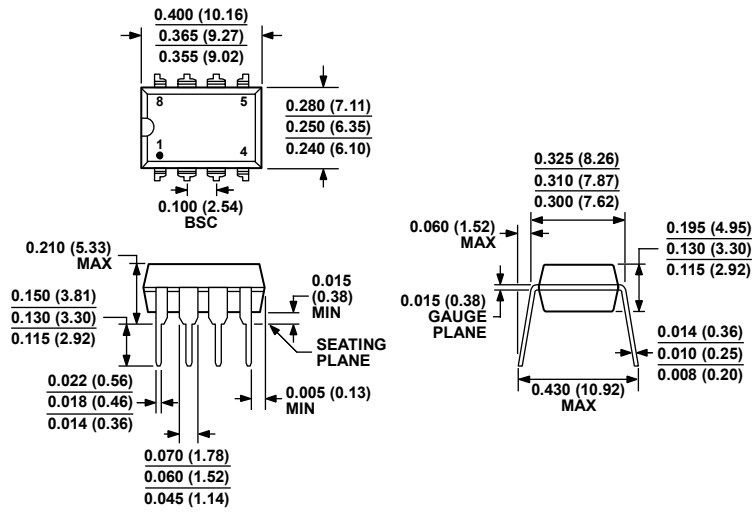
ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

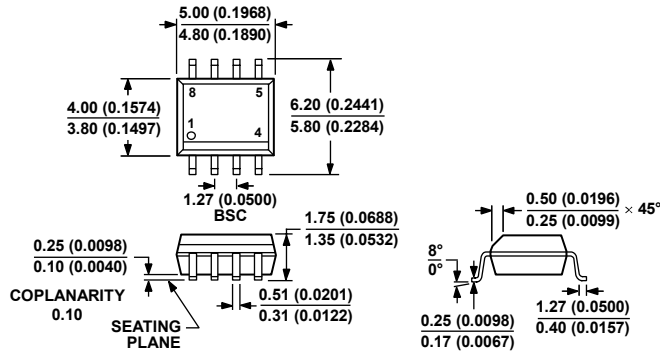
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-001
 CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 54. 8-Lead Plastic Dual In-Line Package [PDIP] Narrow Body (N-8)

Dimensions shown in inches and (millimeters)



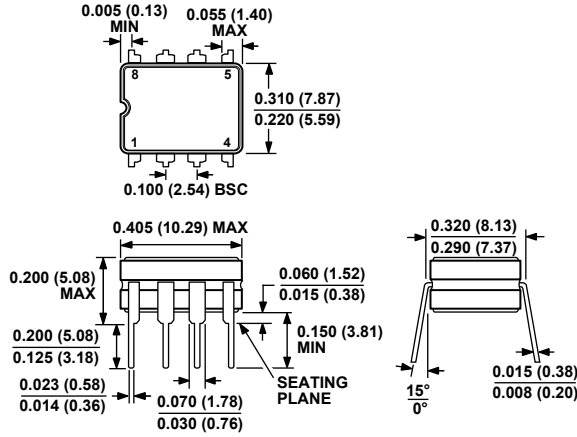
COMPLIANT TO JEDEC STANDARDS MS-012-AA
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 55. 8-Lead Standard Small Outline Package [SOIC_N] Narrow Body (R-8)

Dimensions shown in millimeters and (inches)

070606-A

012407-A



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 56. 8-Lead Ceramic Dual In-Line Package [CERDIP] (Q-8)

Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
OP249AZ	-55°C to +125°C	8-Lead CERDIP	Q-8
OP249FZ	-40°C to +85°C	8-Lead CERDIP	Q-8
OP249GP	-40°C to +85°C	8-Lead PDIP	N-8
OP249GPZ ¹	-40°C to +85°C	8-Lead PDIP	N-8
OP249GS	-40°C to +85°C	8-Lead SOIC_N	R-8
OP249GS-REEL	-40°C to +85°C	8-Lead SOIC_N	R-8
OP249GS-REEL7	-40°C to +85°C	8-Lead SOIC_N	R-8
OP249GSZ ¹	-40°C to +85°C	8-Lead SOIC_N	R-8
OP249GSZ-REEL ¹	-40°C to +85°C	8-Lead SOIC_N	R-8
OP249GSZ-REEL7 ¹	-40°C to +85°C	8-Lead SOIC_N	R-8

¹ Z = RoHS Compliant Part.

For Military processed devices, see the standard microcircuit drawings (SMD) available at

Table 7.

SMD Part Number	Analog Devices, Inc. Equivalent
5962-9151901M2A	OP249ARCMDA
5962-9151901MPA	OP249AZMDA